a signal generating circuit responsive to the first external signal[,] and said threshold signal[, and said first predetermined voltage] for producing said second signal.

456.(Once Amended) The device of claim 443, additionally comprising a reset circuit interposed between said first and second circuits for receiving said first output signal from said first circuit and for terminating said first output signal when predetermined stability requirements are not [meet] met.

Please add the following new claims.

466. A device for controlling the powering up of a first voltage supply, comprising:

a first voltage detector constructed of substantially identical p-channel and n-channel devices for producing a first output signal indicative of a first external signal being greater than a predetermined voltage substantially independently of process variations;

a reset circuit responsive to said first voltage detector for outputting said first output signal when said first external signal is stable;

a logic circuit responsive to said reset circuit and a second external signal; and

a latch responsive to said logic circuit for producing a first enable signal for controlling the powering up of a first voltage supply.

467. The device of claim 466 wherein said reset circuit comprises:

a plurality of series-connected buffers with a first one of said buffers responsive to said first output signal; and

a logic circuit responsive to said first output signal and a last one of said series-connected buffers.

468. The device of claim 467 wherein said reset circuit is constructed such that the first external signal must remain within a predetermined range for approximately one hundred nanoseconds for said logic circuit to output said first output signal.

469. A device for controlling the powering up of a first voltage supply, comprising:

a first voltage detector comprised of p-channel devices for producing a first signal indicative of a first external signal being greater than a first predetermined voltage;

a second voltage detector comprised of n-channel devices for producing a second signal indicative of the first external signal being greater than said first predetermined voltage;

a logic circuit responsive to said first and second signals for producing a first output signal;

a reset circuit responsive to said first output signal;

a logic circuit responsive to said reset circuit and a second external signal; and